# Anomalous Behavior of Gate Current and TDDB Lifetime by Constant Voltage Stress in NO-annealed SiC-MOSFETs

Eiichi Murakami, Member, IEEE and Mitsuo Okamoto

Abstract-Silicon-carbide metal oxide semiconductor field effect transistors (SiC-MOSFETs) are core devices for future power electronics. The factors limiting their automotive applications are currently under investigation. Post-oxidation annealing in NO gas is a key technology to achieving high carrier mobility in SiC-MOSFETs. Herein, we study NO annealing effects on time-dependent dielectric breakdown (TDDB) reliability by constant voltage stress (CVS) method at room temperature. We show that heavy NO annealing enhances hole trapping near the SiO<sub>2</sub>/SiC interface and leads to a rapid increase in the gate current  $(I_g)$ , and results in shorter time-to-breakdown ( $t_{BD}$ ), and smaller Weibull slope of  $t_{BD}$  in comparison to light NO annealing case. However, the detailed examination of the  $I_g$  behavior reveals that the charge -to-breakdown  $(Q_{BD})$  and its distribution do not deteriorate. Therefore, we must reconsider the use of the CVS method by examining the Ig behavior during stress, which strongly depends on NO annealing conditions.

*Index Terms*— charge-to-breakdown, constant voltage stress, NO annealing, SiC-MOSFETs, TDDB, time-to-breakdown.

#### I. INTRODUCTION

S ilicon-carbide metal oxide semiconductor field effect transistors (SiC-MOSFETs) are core devices for future power electronics such as in railway and automotive applications. Post-oxidation annealing by NO gas is a key technology availing SiC-MOSFETs for use. The drastic improvement in carrier mobility [1][2] and its impact on reliability such as positive-bias temperature instability (PBTI) and negative-bias temperature instability (NBTI) are well-known [2][3]. Relatively heavy NO annealing conditions can suppress PBTI and can enhance NBTI. However, it has been reported that commercially available SiC-MOSFETs have different BTI characteristics [4], which suggests different NO annealing conditions.

Recently, time-dependent dielectric breakdown (TDDB) of commercially available SiC-MOSFETs has been investigated to advance their large-scale production for automotive use [5]. The constant voltage stress (CVS, [6]) method is widely used to guarantee gate oxide integrity (GOI). We compared CVS-TDDB characteristics of commercially available SiC-MOSFETs [7]. By combining with BTI data, we speculated that heavy NO annealing

(e-mail: eiichi@ip.kyusan-u.ac.jp).

conditions result in a wider lifetime distribution (or a smaller shape parameter of the Weibull plot for TDDB time-to-breakdown ( $t_{BD}$ ) [6][8]) and a larger number of extrinsic failures (or B-modes [9][10]). It should be noted that both SiC-MOSFETs are not of the latest vintage and are not for automotive use. They have vertical planar MOSFET structure with 45–46-nm-thick gate-oxides (measured by a transmission electron microscope). A lack of knowledge on the process flow of these devices and the above observations motivated this study.

Moreover, there have been few studies on nitridation effects on TDDB other than those by Fujihira et al. [11] and Senzaki et al. [12], which were based on constant current stress (CCS, [6]) method. Additionally, CVS has been argued to be inappropriate for separating B-modes [13]. However, the reason has not been clarified yet, and the actual operation is controlled by voltage. Thus, the CVS method should be more precisely examined, as done by a previous study on Si-MOSFETs with thick oxides [14].

The purpose of this study is to clarify the NO annealing effects on TDDB characteristics using chips for test element groups (TEG) fabricated by known processes. The CVS method is used in combination with the gate current ( $I_g$ ) and the drain current ( $I_{ds}$ ) measurements that can detect electron and hole trapping behaviors during stress. In addition, we attempt to suggest the effects of nitrogen on the B-mode mechanism for further study.

#### II. EXPERIMENT AND MODELING

We used lateral SiC-MOSFETs with 50-nm gate oxide thicknesses ( $t_{ox}$ ), 5- and 100-µm gate-lengths ( $L_g$ ), and 200-µm gate-widths ( $W_g$ ). Samples were annealed under different NO conditions at 1250 °C for 10 min (NO10) and for 60 min (NO60). For NO60, the areal nitrogen density reaches the saturation level [15] at  $3.5 \times 10^{14} \ cm^{-2}$  [16]. For NO10, the density is approximately 1/6 of this saturation level [15]. These samples were fabricated by the National Institute of Advanced Industrial Science and Technology (AIST). It has been reported that NO60 samples have higher field-effect mobility owing to interface trap reduction [17].

First, we compared the initial  $I_{g}$ - $V_{gs}$  and  $I_{ds}$ - $V_{gs}$ @  $V_{ds}$ =50 mV characteristics of SiC-MOSFETs. A conventional source measure unit (Keysight B2902A) was used, and all measurements were performed at room temperature. Double-sweep measurement mode was used to check the hysteresis in  $I_{g}$ - $V_{gs}$  and  $I_{ds}$ - $V_{gs}$  characteristics. Then, CVS tests were performed, during which  $I_{g}$ - $V_{gs}$  and  $I_{ds}$ - $V_{gs}$  characteristics were measured to monitor electron and hole

E. Murakami is with Department of Electrical Engineering, Faculty of Science and Engineering, Kyushu Sangyo University, Matsukadai, Fukuoka-shi, Fukuoka, 813-8503, Japan.

M. Okamoto is with National Institute of Advanced Industrial Science and Technology (AIST), Umezono, Tsukuba, Ibaraki 305-8568, Japan (e-mail: mitsuo-okamoto@aist.go.jp).

trapping. SiC-MOSFETs with  $L_g=5 \mu m$  and 100  $\mu m$  were used for area-scaled Weibull plots [18][6].

In addition, the anomalous  $I_g$  behavior was modeled using a Wentzel-Kramers-Brillouin (WKB) calculation [19] for the tunneling coefficient of the electrons.

# III. RESULTS AND DISCUSSION

#### A. Gate-Current Behavior

The initial  $I_g$ - $V_{gs}$  and  $I_{ds}$ - $V_{gs}$  characteristics of SiC-MOSFETs ( $L_g = 100 \ \mu$ m) are shown in Fig.1. The NO60 sample shows a much larger  $I_g$  than NO10. The  $I_g$ - $V_{gs}$ characteristics show a departure from the theoretical Fowler-Nordheim curve above 42 V (Fig. 1(a)). The double-sweep measurements ( $-10 \ V \rightarrow 47 \ V \rightarrow -10 \ V$ ) clearly indicate a negative shift in threshold voltage ( $V_{th}$ ) (Fig. 1(b)) as well as an increase in  $I_g$  in the downward sweep. These observations mean that hole trapping occurred in the upward sweep up to 47 V. Based on the vast knowledge of the SiO<sub>2</sub>/Si system [20], an oxide electric field near 10 MV/cm can induce impact ionization in the 50-nm-thick oxide layer and make the generation of holes possible.

Furthermore, we have confirmed that the gate current above 42 V depends on  $V_{gs}$ -sweep rate, suggesting an additional hole-trapping during the  $V_{gs}$ -sweep. Thus, we primarily focus on the  $I_g$  values obtained from 25 V to 40 V for analyzing  $I_g$ - $V_{gs}$  characteristics.



Fig. 1 Measured initial  $I_g$ - $V_{gs}$  (a)(c) and  $I_{ds}$ - $V_{gs}@V_{ds}$ =50 mV (b)(d) characteristics of SiC-MOSFETs annealed under NO60 (a)(b) and NO10 (c)(d) conditions, respectively. Double-sweep measurement mode (-10 V $\rightarrow$  47V(NO60), 49 V(NO10)  $\rightarrow$ -10 V) was used to check the hysteresis at room temperature. NO60 sample shows clear hysteresis suggesting hole-trapping near the SiO<sub>2</sub>/SiC interface. The estimated trapped-hole density from  $\Delta V_{th}$  is 1.7 × 10<sup>12</sup> cm<sup>-2</sup>.

Moreover, we measured bi-directional  $I_g$ - $V_{gs}$  characteristics [21] and negligible  $I_g$  changes in the negative  $V_{gs}$  region suggesting that the trapped-holes are located near the SiO<sub>2</sub>/SiC interface. The number of trapped holes ( $N_{ot}^+$ ) is estimated to be  $1.7 \times 10^{12}$  cm<sup>-2</sup> using the equation

$$N_{ot}^{+} = -\frac{c_{ox}}{q} \Delta V_{th} \tag{1}$$

where q is the electronic charge,  $C_{ox}$  is the oxide capacitance per unit area, and  $\Delta V_{th}$  is the threshold voltage shift.

On the other hand, the NO10 sample shows no remarkable hysteresis (Fig. 1(c) and (d)) including under the higher maximum  $V_{gs}$  (-10 V $\rightarrow$ 49 V $\rightarrow$ -10 V). The hole trapping must be originated from high-concentrated nitrogen near the SiO<sub>2</sub>/SiC interface in the NO60 sample.

Figure 2 shows  $I_g$ - $V_{gs}$  and  $I_{ds}$ - $V_{gs}$  characteristics during a CVS test for similar samples. An NO60 sample shows an initial increase and subsequent gradual decrease in  $I_g$ , in contrast to the gradual continuous increase in the NO10



Fig. 2 Measured  $I_{g}$ - $V_{gs}$  (a)(c) and  $I_{ds}$ - $V_{gs}$  @  $V_{ds}$ =50 mV (b)(d) characteristics during  $V_{gs}$ -stress for NO60 (a)(b) and NO10 (c)(d) samples, respectively. NO60 sample shows a rapid increase and subsequent gradual decrease in  $I_{gs}$ , in contrast to the gradual continuous increase in NO10 sample. This anomalous  $I_{g}$  behavior can be explained by hole and electron trapping with different locations of the charge centroid.

sample. We previously reported the behavior of the NO10 sample for samples from one vendor [22][23] and attributed it to interfacial hole trapping. More recently, we found behavior similar to that of the NO60 sample for samples from the other vendors [7]. Thus, we aim to discuss the details of the behavior of the NO60 samples.

From the  $I_{ds}$ - $V_{gs}$  characteristics, the behavior of  $\Delta V_{th}$  shows electron trapping after hole trapping. Moreover, the  $I_g$ - $V_{gs}$ characteristics are more complicated. Above 42 V, hole trapping during  $V_{gs}$ -sweep is added as discussed in Fig. 1(a) and (b). After 240 s of stress,  $I_g$  at  $V_{gs}$  = 40 V becomes smaller than that of the data for 60 s stress, although  $I_g$  at  $V_{gs}$  = 25 V is very similar. The bi-directional  $I_g$ - $V_{gs}$  data suggest that the electron is near the SiO<sub>2</sub>/SiC interface.

## B. Impact of Hole and Electron Trapping on the Tunneling Transmission Coefficient

This anomalous behavior shown in Fig. 2(a) can be explained by extending the WKB calculation for the hole-trapping case [22][23] to the hole- and electron-trapping

case, where the sheet electron charge is assumed to be nearer to the  $SiO_2/SiC$  interface than that of the hole.

As shown in Fig.3, first, the holes and electrons were assumed to be located at  $d_h$  and  $d_e$  from the SiO<sub>2</sub>/SiC interface as their areal densities  $N_{ot}^+$  and  $N_{ot}^-$ , respectively.  $\Delta V_{th}$  can be expressed as follows [21]:

$$\Delta V_{th} = -\frac{qN_{ot}^+}{c_{ox}} \left(1 - \frac{d_h}{t_{ox}}\right) + \frac{qN_{ot}^-}{c_{ox}} \left(1 - \frac{d_e}{t_{ox}}\right).$$
(2)

Using Gauss law, the electric fields in SiO<sub>2</sub> ( $E_{ox1}$ ,  $E_{ox2}$ ,  $E_{ox3}$ ) can be calculated to obtain the potential energy for the electrons (U(x)). Finally, the electron tunneling transmission coefficient (D) can be calculated using the so-called Gamow penetration factor shown in Eq.(3) [19].



Fig. 3 An illustration of hole- and electron-trapping location and electric fields in  $SiO_2$ . The charge centroid of electron is assumed to be shallower than that of the holes which can explain the gross behavior of the experimental results.

$$D = \exp\left(-\frac{2}{\hbar}\int_0^{x_t}\sqrt{2m^*(U(x) - E)}\,dx\right) \tag{3}$$

where,  $\hbar$  is the Planck constant,  $x_t$  is the tunneling distance,  $m^*$  is the effective electron mass ( $m^*=0.42 m_0$  (free electron mass) [24]), and *E* is the energy of the electron. (See the Appendix for calculation details.)



Fig. 4 Calculated U(x)-*E* for Vgs=25 V (a) and Vgs=40 V (b), and transmission coefficient *D* of tunneling electron (c). The same data in Fig. 2(a) are shown as (d) from  $V_{\rm gs} = 25$  V to  $V_{\rm gs} = 40$ V where hole trapping during  $V_{\rm gs}$ -sweep is negligible.

Fig. 4 (a) and (b) show the calculated U(x)-*E* at  $V_{gs}$ =25 V and 40 V, respectively.  $U_0$  means initial state,  $U_h$  means only hole trapping corresponding to 60-s data in Fig.2 (a), and  $U_{he}$  means both electron and hole trapping corresponding to the 240-s data in Fig.2 (a).

The parameters in the model (Table I) were estimated by comparing the calculated *D* with  $I_g$ , as shown in Fig.4(c) and (d) as well as  $\Delta V_{th}$ . This model can express the anomalous behavior of  $I_g$ - $V_{gs}$  characteristics qualitatively. It should be noted that  $d_e$  is smaller than  $d_h$ . At  $V_{gs}=25$  V, hole trapping at  $d_h$ , which reduces  $x_t$  and enhances the tunneling, has a dominant effect. In contrast, at  $V_{gs}=40$  V,  $x_t$  is located near  $d_e$ , thus, electron trapping which retards tunneling, is more effective.

ΓА	BI	Æ	1
	~ ~	_	

Model parameters used in the calculation in Fig. 4(a)(b)(c).

d <sub>h</sub> (cm)	5.7E-07
d <sub>e</sub> (cm)	1.4E-07
Not <sup>+</sup> @60 s (cm <sup>-2</sup> )	3.4E+12
Not <sup>+</sup> @240 s (cm <sup>-2</sup> )	6.8E+12
Not <sup>-</sup> @60s (cm <sup>-2</sup> )	0
Not <sup>-</sup> @240 s (cm <sup>-2</sup> )	7.1E+12

In this analysis, we modeled the  $I_g$ - $V_{gs}$  characteristics by modifying the Fowler-Nordheim tunneling using trapped holes and electrons. It should be noted that Pool-Frenkel [25] or trap-assisted tunneling [26] mechanism should be considered in the low  $V_{gs}$  region even at RT. This examination is for further study.

### C. TDDB Characteristics by CVS

In Fig. 5, Weibull plots are shown where the stress  $V_{gs}$  voltages were 47 V for the NO60 sample and 49 V for the NO10 sample. The vertical axis is the cumulative defect density defined as follows [6]:

$$D(t) \equiv -\ln\left(1 - F(t)\right)/A \tag{4}$$

where F(t) is the cumulative failure calculated using the median ranks [8] and  $A = L_g W_g$  is the gate-oxide area. The formation of oxide defects seems random, and a Poisson distribution is assumed.  $A = 1 \times 10^{-5}$  and  $2 \times 10^{-4}$  for the samples with  $L_g = 5 \mu m$  and  $L_g = 100 \mu m$ , respectively. Clear universal plots were obtained for both samples, validating the Poisson distribution. In other words, area-scaling as in [18][6] was verified. The shape parameter (*m*) of the NO60 samples is approximately half that of the NO10 samples, where the following Weibull distribution is assumed [8].

$$F(t) \equiv 1 - e^{-\left(\frac{t}{c}\right)} \tag{5}$$

where c is the characteristic life and m is the shape parameter.

In Fig. 6, the time-dependent  $I_g$  at the stress  $V_{gs}$  is plotted for all the samples with  $L_g=5 \ \mu\text{m}$ . The time dependence is mainly universal immediately before the breakdown. The rapid decrease in  $I_g$  after the breakdown is probably due to electrically open gate electrodes in the majority of the samples. The NO60 samples show much greater  $I_g$  at stress  $V_{gs}$ . Charge-to-breakdown ( $Q_{BD}$ ) can be estimated by integrating the  $I_g$  from 0 to the  $t_{BD}$ . This  $Q_{BD}$  value is much larger in the NO60 sample. As shown in Fig. 6(a),  $Q_{BD}$  is determined approximately at the initial increase phase of  $I_g$ . Thus, the distribution of  $Q_{BD}$  becomes much steeper than that of  $t_{BD}$  in the NO60 sample. In fact, for samples with  $L_g=5 \ \mu\text{m}$ ,  $t_{BD}^{\text{max}}/t_{BD}^{\text{min}}$  is 3.4 and 1.7, however,  $Q_{BD}^{\text{max}}/Q_{BD}^{\text{min}}$  is 1.2 and 1.9, for NO60 and NO10 samples, respectively.





Fig. 5 Area-scaled Weibull plots for  $t_{BD}$  by CVS in which stress  $V_{gs}$  voltages was 47 V for the NO60 samples (a), and 49 V for the NO10 ones (b), respectively. Each data point with error bar (9 data for  $L_g = 5$  µm and 6 data for  $L_g = 100$  µm) corresponds to  $t_{BD}$  of measured sample. Then, the triangle and circle plots mean cumulative defect density as a function of stress time, for  $L_g = 5$  µm and 100 µm, respectively. Weibull parameter fitting was performed including both  $L_g$ . The Weibull slope of the NO60 samples is approximately half that of the NO10 samples.

There are several reports on TDDB distributions by CCS measurements [11]-[13] in which Weibull plots for  $Q_{BD}$  are used. Lifetime enhancement effects have been discussed in [11][12], and good lifetime distributions for many samples have been demonstrated [13]. Although our data show that  $t_{BD}$  is not improved by heavy nitridation both in its lifetime and distribution, the obtained information on  $Q_{BD}$  does not contradict these previous results.

These results seem to be consistent with the "charging-induced dynamic stress" concept proposed by Okada et al. [14], where  $Q_{BD}$  is a physical measure of oxide quality [27]. When  $I_g$  is in the decreasing phase [14], a sample with a larger  $Q_{BD}$  shows a much larger  $t_{BD}$  by CVS than expected. On the contrary, in the increasing phase, a sample with larger  $Q_{BD}$  suffers stronger stress than expected; thus,

Fig. 6 Time-dependent  $I_g$  at the stress  $V_{gs}$  for all the samples with  $L_g=5 \ \mu m (9)$  devices for each condition), (a)NO60 (b) NO10. The time dependence is mainly universal immediately before the breakdown. The rapid decrease in  $I_g$  after the breakdown is probably because of electrically open gate-electrode in the majority of the samples. The NO60 samples show much greater  $I_g$  at stress  $V_{gs}$  and as a result larger  $Q_{BD}$ . The  $Q_{BD}$  of NO60 samples are determined by the initial increasing phase of  $I_g$ . Thus, the  $Q_{BD}$  distribution becomes much steeper than  $t_{BD}$ .

reducing its  $t_{BD}$ . The former corresponds to the NO60 sample and the latter corresponds to the NO10 sample in our data.

Moens et al. [26] reported that the increasing phase is altered to the decreasing phase when the gate electric-field falls below 9.0 MV/cm. More interestingly, this phenomenon leads to a bi-modal Weibull distribution at 9.3 MV/cm. Therefore, we believe that this "charging-induced dynamic stress" concept is essential for TDDB analysis of SiC-MOSFETs.

The Poisson distribution of nitrogen atoms indicating pure randomness suggests the possibility of locally higher nitrogen concentration, which might be the cause of the oxide weak spot leading to a wider  $t_{BD}$  distribution. However, based on the above discussion, an experimentally observed wider  $t_{BD}$  distribution can be explained [14]. Thus, this is probably not the case.

Another speculation relating to nitrogen is that heavy NO annealing samples have large numbers of B-mode as indicated in the introduction. In the present study, we observed a few B-modes for NO60 samples of another batch. As far as we know, a crystal-defect originated mechanism [28] is dominant for B-modes, and a threading screw dislocation (TSD) has been reported to be a killer defect [29]. In the vicinity of the TSD, crystal facets other than the Si-face ((0001) surface) are formed [30], and these surfaces can capture more nitrogen atoms [16]. The XPS studies of the nitridation of several crystal faces [31] have shown that C-, a-, and m-faces have approximately two times higher nitrogen concentration than the Si-face. As a result, the local nitrogen cluster surrounding TSD may cause a weak spot of the oxide, which is similar to the mechanism of local hole-trapping in SiO<sub>2</sub>/Si studies [32]. Thus, heavy NO annealing may lead to B-mode failures. However, this hypothesis requires more extensive study.

#### V. CONCLUSIONS

Heavy NO annealing complicates the  $I_g$  behavior at high  $V_{gs}$ , which can be explained by hole and electron trapping near the SiO<sub>2</sub>/SiC interface. Moreover, it reduces  $t_{BD}$  and widens its distribution. However,  $Q_{BD}$  as a physical measure of oxide quality does not deteriorate. As a method for GOI, CVS must be considered by examining the  $I_g$  behavior during stress. At present, the use of  $Q_{BD}$ -based method seems preferable for the analysis of heavy NO annealed samples.

### Appendix

This appendix contains details of the calculations for the electron-tunneling coefficient based on Gauss law and the WKB approximation.

The basic electrostatic equations including Gauss law are as follows.

$$V_{gs} - V_{FB} = V_{ox} + 2\psi_B \tag{A1}$$

$$V_{ox} = E_{ox1}d_e + E_{ox2}(d_h - d_e) + E_{ox3}(t_{ox} - d_h)$$
(A2)  
$$E_{ox1} - E_{ox2} = -\frac{Q_{ot}}{Q_{ot}}$$
(A3)

$$L_{0x1} = L_{0x2} = -\frac{1}{\epsilon_0 \epsilon_{0x}}$$
(A3)

$$E_{ox2} - E_{ox3} = \frac{Q_{ot}}{\epsilon_0 \epsilon_{ox}} \tag{A4}$$

where  $V_{\rm FB}$  is the flat-band voltage,  $V_{\rm ox}$  is the potential drop across the oxide,  $\psi_{\rm B}$  is the difference between Fermi potential and intrinsic potential,  $Q_{\rm ot}$  is the oxide-trapped-electron per unit area (=q $N_{\rm ot}$ ),  $Q_{\rm ot}$  is the oxide-trapped-hole per unit area (=q $N_{\rm ot}$ ),  $\epsilon_0$  is the vacuum permittivity, and  $\epsilon_{ox}$  is the relative oxide permittivity.

These equations can be rewritten in matrix form.

$$\begin{bmatrix} d_e & d_h - d_e & t_{ox} - d_h \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} E_{ox1} \\ E_{ox2} \\ E_{ox3} \end{bmatrix} = \begin{bmatrix} v_{ox} \\ -\frac{Q_{ot}}{\epsilon_0 \epsilon_{ox}} \\ \frac{Q_{ot}}{\epsilon_0 \epsilon_{ox}} \end{bmatrix}$$
(A5)

By introducing,

$$E_{ox0} \equiv \frac{V_{gs} - V_{FB} - 2\psi_B}{t_{ox}} \tag{A6}$$

which is the average field in the oxide, and  $\Delta E_{oxi} \equiv E_{oxi} - E_{ox0} \quad (i=1, 2, 3), \quad (A7)$   $\begin{bmatrix} d_e & d_h - d_e & t_{ox} - d_h \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} \Delta E_{ox1} \\ \Delta E_{ox2} \\ \Delta E_{ox3} \end{bmatrix} = \begin{bmatrix} 0 \\ -\frac{Q_{ot}}{\varepsilon_0 \epsilon_{ox}} \\ \frac{Q_{ot}}{\varepsilon_0 \epsilon_{ox}} \end{bmatrix}$ (A8)

As a result, the solutions for the electric fields are

$$\Delta E_{ox1} = \left(1 - \frac{d_h}{t_{ox}}\right) \frac{Q_{ot}^+}{\epsilon_0 \epsilon_{ox}} - \left(1 - \frac{d_e}{t_{ox}}\right) \frac{Q_{ot}^-}{\epsilon_0 \epsilon_{ox}}$$
(A9)

$$\Delta E_{ox2} = \left(1 - \frac{d_h}{t_{ox}}\right) \frac{Q_{ot}^+}{\epsilon_0 \epsilon_{ox}} + \frac{d_e}{t_{ox} \epsilon_0 \epsilon_{ox}} \tag{A10}$$

$$\Delta E_{ox3} = -\frac{d_h}{t_{ox}} \frac{Q_{ot}^+}{\epsilon_0 \epsilon_{ox}} + \frac{d_e}{t_{ox}} \frac{Q_{ot}^-}{\epsilon_0 \epsilon_{ox}}$$
(A11)

By integrating the electric fields, the potential energy for electrons is calculated.

$$U(x) - E = q(\phi_{ox} - E_{ox1}x) \equiv G_1(x) : 0 < x < d_e = q\{\phi_{ox} - [E_{ox1}d_e + E_{ox2}(x - d_e)]\} \equiv G_2(x) : d_e < x < d_h = q\{\phi_{ox} - [E_{ox1}d_e + E_{ox2}(d_h - d_e) + E_{ox3}(x - d_h)]\} \equiv G_3(x) : x > d_h$$
(A12)

where  $\phi_{ox}$  is the SiC-SiO<sub>2</sub>interface potential barrier for electrons.

Using the Gamow penetration factor (3), the following are the results for D.

Case A: 
$$U(d_e) < E$$
  
 $x_t = \frac{\phi_{ox}}{E_{ox1}} < d_e$  (A13)

$$D = exp\left(-\frac{2\sqrt{2m^*}}{\hbar}\int_0^{x_t}\sqrt{G_1(x)} dx\right)$$
$$= exp\left(-\frac{C\phi_0x^{3/2}}{E_{\text{out}}}\right)$$
(A14)

$$C \equiv \frac{4\sqrt{2m^*q}}{3\hbar} \tag{A15}$$

Case B: 
$$U(d_e) > E$$
 and  $U(d_h) < E$   
 $d_e < x_t = d_e + \frac{\phi_{ox} - E_{ox1}d_e}{E_{ox2}} < d_h$  (A16)  
 $= \left( \frac{2\sqrt{2m^*} \left[ cd_e \sqrt{2m^*} \right] + cd_e}{2m^*} \right)$ 

$$D = exp\left\{-\frac{2\sqrt{2m^{2}}}{\hbar}\left[\int_{0}^{d_{e}}\sqrt{G_{1}(x)}\,dx + \int_{d_{e}}^{x_{t}}\sqrt{G_{2}(x)}\,dx\right]\right\}$$
(A17)

$$\therefore D = exp\left[-\frac{C\phi_{ox}^{3/2}}{E_{ox1}}(1+\alpha)\right]$$
(A18)

$$\alpha \equiv \left(\frac{E_{ox1}}{E_{ox2}} - 1\right) \left(1 - \frac{E_{ox1}d_e}{\phi_{ox}}\right)^{3/2}$$
(A19)

$$Case C: U(d_{h}) > E d_{h} < x_{t} = d_{e} + \frac{\phi_{ox} - E_{ox1}d_{e} - E_{ox2}(d_{h} - d_{e})}{E_{ox3}} < t_{ox} D = exp \left\{ -\frac{2\sqrt{2m^{*}}}{\hbar} \left[ \int_{0}^{d_{e}} \sqrt{G_{1}(x)} \, dx + \int_{d_{e}}^{d_{h}} \sqrt{G_{2}(x)} \, dx + \int_{d_{h}}^{x_{t}} \sqrt{G_{3}(x)} \, dx \right] \right\}$$
(A20)

$$(A21)$$

$$(A21)$$

$$(A22)$$

$$\beta \equiv \left(\frac{E_{ox1}}{E_{ox3}} - \frac{E_{ox1}}{E_{ox2}}\right) \left(1 - \frac{E_{ox1}d_e + E_{ox2}(d_h - d_e)}{\phi_{ox}}\right)^{3/2}$$
(A23)

the equations become easier to solve.

### ACKNOWLEDGMENT

We would like to thank Dr. Kiminori Hamada of PDPlus LLC for encouraging to start this study at ICSCRM 2019.

#### REFERENCES

- G. Y. Chung, C. C. Tin, and J. R. Williams, "Improved Inversion Channel Mobility for 4H-SiC MOSFETs Following High Temperature Anneals in Nitric Oxide," *IEEE Electron Device Lett.* Vol. 22, pp. 176-178, April 2001, doi:10.1109/55.915604.
- [2] J. Rosen, S. Dhar, M. E. Zvanut, J. R. Williams, and L. C. Feldman, "Density of interface states, electron traps, and hole traps as a function of as a function of the nitrogen density in SiO<sub>2</sub> on SiC," *J. Appl. Phys.* 105, pp.124506 1-11, 2009, doi:10.1063/1.3131845.
- [3] D. Okamoto, H. Nemoto, X. Zhang, X. Zhou, M. Sometani, M. Okamoto, S. Harada, T. Hatakeyama, N. Iwamuro, and H. Yano, "Threshold Voltage Instability in p-channel 4H-SiC MOSFETs Investigated by Non-relaxation Method," *in Proc. ICSCRM 2019*, Fr-1A-02.
- [4] R. Green, A. Lelis, and D. Habersat, "Threshold-voltage bias -temperature instability in commercially-available SiC MOSFETs," *Jpn*, *J. Appl. Phys.* 55, pp. 04EA03 1-8, 2016, doi:10.7567/JJAP.55.04EA03.
- [5] T. Liu, S. Zhu, S. Yu, D. Xing, A. Salemi, M. Kang, K. Booth, M. H. White, and A. K. Agarwal, "Gate Oxide Reliability Studies of Commercial 1.2 kV 4H-SiC Power MOSFETs," *in Proc. Int. Rel. Phys. Symp.*, 2020, doi:10.1109/IRPS45951.2020.9129486.
- [6] E. Y. Wu, R. P. Vollertsen, and J. Sune, "Dielectric Characterization and Reliability Methodology," in Reliability Wearout Mechanism in Advanced CMOS Technologies, New Jersey: IEEE Press/ Wiley, 2009, pp.71-208.
- [7] R. Tanaka, K. Terano, and H. Harano, Bachelor thesis of Kyushu Sangyo University 2019, unpublished.
- [8] P. A. Tobias and D. C. Trindade, *Applied Reliability second edition*, New York: Chapman & Hall/CRC, 1998, pp. 81-165.
- [9] K. Yamabe and K. Taniguchi, "Time-dependent-dielectric-breakdown of thin thermally grown SiO<sub>2</sub> films," *IEEE Trans. Electron Devices* vol. 32, pp. 423-428, Feb. 1985, doi:10.1109/T-ED.1985.21958.
- [10] N. Suzumura, M. Ogasawara, K. Makabe, T. Kamoshima, T. Ouchi, T. Furusawa, and E. Murakami, "Comprehensive TDDB lifetime prediction methodology for intrinsic and extrinsic failures in Cu interconnect dielectrics," *Microelectron. Eng.* 106, pp. 2000-2004, 2013, doi:10.1016/j.mee.2013.01.015.
- [11] K. Fujihira, N. Miura, K. Shiozawa, M. Imaizumi, K. Ohtsuka, and T. Takami, "Successful Enhancement of Lifetime for SiO<sub>2</sub> on 4H-SiC by N<sub>2</sub>O Anneal," *IEEE Electron Device Lett.* Vol. 25, pp. 734-736, Nov. 2004, doi:10.1109/LED.2004.837533.
- [12] J. Senzaki, A. Shimozato, K. Kojima, T. Kato, Y. Tanaka, K. Fukuda, and H. Okumura, "Challenges of high-performance and high-reliability in SiC MOS structures," *Mater. Sci. Forum*, 717, pp.703-708, 2012, doi:10.4028/www.scientific.net/MSF.717-720.703.
- [13] M. Sagawa, H. Miki, Y. Mori, H. Shimizu, and A. Shima, "Evaluation of Gate Oxide Reliability in 3.3 kV 4H-SiC DMOSFET with J-Ramp TDDB Methods," *in Proc.* 30<sup>th</sup> Int. Symp. PSDIC, pp. 363-366, 2018, doi:10.1109/ISPSD.2018.8393678.
- [14] K. Okada, K. Kurimoto, and M. Suzuki, "Anomalous TDDB Statistics of Gate Dielectrics Caused by Charging-Induced Dynamic Stress Relaxation Under Constant-Voltage Stress," *IEEE Trans. Electron Devices*, vol. 63, pp. 2268-2274, June 2016, doi:10.1109 /TED.2016.2549555.
- [15] K. Moges, M. Sometani, T. Hosoi, T. Shimura, S. Harada, and H. Watanabe, "Sub-nanometer-scale depth profiling of nitrogen atoms in SiO<sub>2</sub>/4H-SiC structures treated with NO annealing," *Appl. Phys. Express*, pp. 101303 1-4, 2018, doi:10.7567/APEX.11.101303.
- [16] S. Dhar, L. C. Feldman, K.-C. Chang, Y. Yao, L. M. Porter, J. Bentley, and J. R. Williams, "Nitridation anisotropy in SiO<sub>2</sub>/4H-SiC," *J. Appl. Phys.* 97, pp. 074902 1-6, 2005, doi:10.1063/1.1863423.
- [17] T. Hatakeyama, Y. Kikuchi, M. Sometani, S. Harada, D. Okamoto, H. Yano, Y. Yonezawa, and H. Okumura, "Characterization of traps at nitrided SiO<sub>2</sub>/SiC interfaces near the conduction band edge by using Hall effect measurements," *Appl. Phys. Express*, 10, pp. 046601 1-4, 2017, doi:10.7567/APEX.10.046601.
- [18] J. Senzaki, A. Shimazato, M. Okamoto, K. Kojima, K. Fukuda, H. Okumura, and K. Arai, "Evaluation of 4H-SiC Thermal Oxide Reliability Using Area-Scaling Method," *Jpn. J. Appl. Phys.* 48, pp. 081404 1-4, 2009, doi:10.1143/JJAP.48.081404.
- [19] L. D. Landau and E. M. Lifshitz, *Quantum Mechanics 3<sup>rd</sup> ed.*, Oxford: Butterworth-Heinemann, 1977, pp. 164-185.

- [20] D. J. DiMaria, E. Cartier, and D. Arnold, "Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon," *J. Appl. Phys.* 73, pp. 3367-3384, 1993, doi:10.1063/1.352936.
- [21] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, "Characterization of Simultaneous Bulk and Interface High-field Trapping Effects in SiO<sub>2</sub>," *in IEDM Tech. Dig.*, Dec. 1983, pp. 182-185, doi: 10.1109/IEDM.1983.190471.
- [22] E. Murakami, T. Takeshita, and K. Oda, "TDDB Lifetime Enhancement in SiC-MOSFETs under Gate-Switching Operations," *Mater. Sci. Forum* 1004, pp. 665-670, 2020, doi:10.4028/www.scientific.net/MSF. 1004.665.
- [23] E. Murakami, K. Oda, and T. Takeshita, "Special features of Fowler-Nordheim stress degradation of SiC-MOSFETs," *Jpn. J. Appl. Phys.* 55, pp. 04ER14 1-6,2016, doi:10.7567/JJAP.55.04ER14.
- [24] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO<sub>2</sub>," J. Appl. Phys. 40, pp.278-283, 1969, doi:10.1063/1.1657043.
- [25] M. Sometani, D. Okamoto, S. Harada, H. Ishimori, S. Takasu, T. Hatakeyama, M. Takei, Y. Yonezawa, K. Fukuda, and H. Okumura, "Temperature-dependent analysis of conduction mechanism of leakage current in thermally grown oxide on 4H-SiC," *J. Appl. Phy.* 117, pp. 024505-1-6, 2015, doi:10.1063/1.4905916.
- [26] P. Moens, J. Franchi, J. Lettens, L. De Schepper, M. Domeji, and F. Allerstam, "A Charge-to-Breakdown (Q<sub>BD</sub>) Approach to SiC Gate Oxide Lifetime Extraction and Modeling," *in Proc.* 32<sup>nd</sup> Int. Symp. PSDIC, pp. 78-81, 2020, doi: 10.1109/ISPSD46842.2020.9170097.
- [27] R. Degraeve, G. Groeseneken, R. Bellens, J. L. Ogier, M. Depas, P. J. Roussel, and H. E. Maes, "New Insights in the Relation Between Electron Trap Generation and the Statistical Properties of Oxide Breakdown," *IEEE Trans. Electron Devices* 45, pp. 904-911, April. 1998, doi:10.1109/16.662800.
- [28] J. Senzaki, K. Kojima, T. Kato, A. Shimazato, and K. Fukuda, "Correlation between reliability of thermal oxides and dislocations in n-type 4H-SiC epitaxial wafers" *Appl. Phys. Lett.* 89, pp. 022909 1-3, 2006, doi:10.1063/1.2221525.
- [29] A. Severino, R. Anzalone, N. Piluso, E. Vitanza, B. Carbone, A. Russo, and S. Coffa, "Impact of Threading Dislocations Detected by KOH Etching on 4H-SiC 650 V MOSFET Device Failure after Reliability Test," *Mater. Sci. Forum* 1004, pp. 472-476, 2020, doi:10.4028/ www.scientific.net/MSF.1004.472.
- [30] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications, Singapore: IEEE Press/Wiley, 2014, pp. 53-54.
- [31] K. Hamada, A. Mikami, H. Naruoka, K. Yamabe, "Analysis of Nitrogen State on MOS Interface of 4H-SiC m-Face after Nitric Oxide Post Oxidation Annealing (NO-POA)," *e-J. Surf. Sci. Nanotech.* 15, pp. 109 -114, 2017, doi:10.1380/ejssnt.2017.109.
- [32] I. C. Chen, S. Holland, and C. Hu, "Electrical Breakdown in Thin Gate and Tunneling Oxides," *IEEE Trans. Electron Devices* 32, pp. 413-422, Feb. 1985, doi:10.1109/JSSC.1985.1052311.